Abstracts

Accurate Nonlinear Transistor Modeling Using Pulsed S Parameters Measurements Under Pulsed Bias Conditions

J.F. Vidalou, J.F. Grossier, M. Chaumas, M. Camiade, P. Roux and J. Oregon. "Accurate Nonlinear Transistor Modeling Using Pulsed S Parameters Measurements Under Pulsed Bias Conditions." 1991 MTT-S International Microwave Symposium Digest 91.1 (1991 Vol. I [MWSYM]): 95-98.

Accurate design of non-linear MICs and MMICs needs accurate modeling of transistors. Two methods are available today, which suffer from several drawbacks: In the first method, S parameters are measured at different DC bias points and a small signal model is extracted with elements depending on bias variables. This method ignores temperature effects due to DC dissipation and cannot be applied to high power transistors. Moreover, it does not allow measurements near the breakdown region. In the second method, the non-linear current sources are extracted from pulsed measurements, and the linear elements from S parameters. However, this method does not allow accurate extraction of the differential elements (such as gm and gd for a FET), moreover this elements cannot be extracted in the pinched region where the pulsed drain current is zero. To overpass all the former drawbacks a new method is proposed which has been applied to FETs modeling: The device is characterized by pulsed S parameters measurements under pulsed bias voltages, in the whole plane of Vgs, Vds, including the breakdown and pinched regions. The resulting transistor model is accurate for all classes of operation: A, AB, B, C; the method may be applied to very high power bipolar transistors used in pulsed class C-radars.

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